

# PATENT ABSTRACTS OF JAPAN

(11)Publication number : 04-114233  
(43)Date of publication of application : 15.04.1992

(51)Int.CI. G06F 7/24  
G06F 15/66  
H04N 1/419  
H04N 7/13

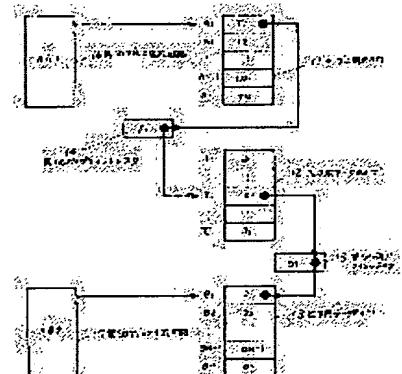
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## (54) DATA ORDER CHANGE CIRCUIT

### (57)Abstract:

PURPOSE: To rearrange data with the small number of cycles by writing the output data of a RAM for table in a pipe-line register, reading out data from a RAM for input with this data as an address, temporarily fetching this data into the pipe-line register and afterwards writing it into a memory for output.

CONSTITUTION: A data is read out from a RAM 11 for table with an address generated by a first address generation circuit 16, and this data is written in a first pipe-line register 14. With the data of the pipe-line register 14 as an address, the data of a RAM 12 for input is read out and this data is written in a pipe-line register 14. In respect to a RAM 13 for output, the data of a second pipe-line register 15 is written in an address generated by a second address generation circuit 17. In this way, the data of the RAM 12 for input is written in the RAM 13 for output while changing the order of the data according to the contents of the RAM 11 for table. Thus, the order of the data can be changed with the almost 1/3 number of cycles in comparison with the conventional data order change circuit.



## LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]